Amendments to the Specification:

Please replace paragraph [0019] with the following amended paragraph:

[0019] If a defect is detected in one or more of the non-redundant memory cells during testing, then either an external test device or the processor 210 may execute a repair algorithm to generate a repair signature to properly allocate the redundant components ~~204~~234 associated with the memory 202 to repair the memory 202. Either an external test device or the processor 210 may cause one or more fuses to signify this defect by changing the fuse's status, and thus, permanently store the location of where the defective non-redundant memory cell was detected. For example, the third fuse 222 is blown indicated by the fuse containing a logical 1; thereby, changing to the fuse's state from an inactive level of a logical 0 to an active logical 1. The third fuse 222 is blown to indicate that one or more non-redundant memory cells in the third group of memory cells 224 coupled to the third input-output circuit 226 are defective.

Please replace paragraph [0021] with the following amended paragraph:

[0021] Figure 3 illustrates a block diagram of an embodiment of a processor having logic configured to test and repair two or more memories electrically connected to that processor. The processor 310 connects to multiple memory arrays, such as the first memory 302 through the Nth number of memory ~~332~~330. The processor 310 also connects to a fuse box 314 that stores a concatenated repair signature that repairs all of the memories connected that processor 310. Each of the memories 302-330 has one or more redundant components associated with that memory. The processor 310 contains redundancy allocation logic to execute one or more repair algorithms to

generate a repair signature for each memory. The repair data container may be a fuse box 314. The fuse box 314 stores actual repair signatures for each memory having one or more defective memory cells and dummy repair signatures for each memory with no defective memory cells. The concatenated repair signature may be an aggregation of all the repair signatures for each of the memories connected to that processor 310. The processor 310 contains logic configured to compose a concatenated repair signature for all of the memories 302-330 sharing the processor 310 and the fuse box 314. The processor 310 composes a concatenated repair signature in order to store that concatenated repair signature in the fuse box 314. The processor 310 also contains logic configured to decompose the concatenated repair signature to send reconfiguration data into all of the memories 302-330 sharing the fuse box 314. The processor 310 also contains logic configured to compress the repair signature when sending bits to be stored in the fuse box 314.

Please replace paragraph [0058] with the following amended paragraph:

[0058] In one embodiment, the software used to facilitate the memory compiler can be embodied onto a machine-readable medium. A machine-readable medium includes any mechanism that provides (e.g., stores and/or transmits) information in a form readable by a machine (e.g., a computer). For example, a machine-readable medium includes read only memory (ROM); random access memory (RAM); magnetic disk storage media; optical storage media; flash memory devices; DVD's, ~~electrical, optical, acoustical or other form of propagated signals (e.g., carrier waves, infrared signals, digital signals~~, EPROMs, EEPROMs, FLASH, magnetic or optical cards, or any type of

media suitable for storing electronic instructions. Slower mediums could be cached to a faster, more practical, medium.